Question 1 Name two techniques to increase parallelism at instruction level

Question 2 T/F In following instructions, OR R7,R1,R8 depends on ADD R1,R1,R6.

ADD R1,R2,R3

BEQ R4,L

ADD R1,R1,R6

L: OR R7,R1,R8

...

Question 3 In a heterogeneous execution model, [CPU] is the host and [GPU] is the device.

Question 4 How would you determine if vector machines would be suitable for a given program?

Question 5 T/F SIMD architectures exploits instruction-level parallelism.

Question 6 T/F Processors with lower CPIs will always be faster.

Question 7 T/F Parallelism at data level means parallel execution of multiple instructions of the same type.

Question 8 Which one of the following processors has the highest possible MIPS rate, assuming full compiler optimization and no cache misses?

A 4-issue processor driven by a 300 MHz clock.

A single-issue processor driven by a 1.2 GHz clock.

A 2-issue processor with a 600 MHz clock.

A 8-issue VLIW processor driven by a 200 MHz clock.

Question 9 [Name] dependency occurs when two instructions use the same register or memory location.

Question 10 When would speculative execution may not be preferable?